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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/657,797 | 09/08/2003 | William C. Moyer | SC13071TH | 1577 |

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| EXAMINER | |
|---|---|
| PAN, DANIEL H | |
| **ART UNIT** | **PAPER NUMBER** |
| 2183 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 12/28/2006 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/657,797 | MOYER ET AL. | |
| | Examiner | Art Unit | |
| | Daniel Pan | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 January 1943*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10,12,13,15-22,25-28 and 30-43* is/are rejected.

7)☒ Claim(s) *8,9,11,14,23,24,26 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :12/05/06,02/09/06, 06/14/05,03/21/05,01/16/04, 09/08/03.

1. Claims 1-43 are presented for examination. TD on 10/24/06 has been received.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2,6,7,10,12,16,17, 19,20,21,25,27 are rejected under 35 U.S.C. 102(b) as being anticipated by Inagami et al. (4,760,545).

3. As to claim 1, 16, Inagami taught at least :

a) a memory for storing operands (see the main storage for storing the vector data elements and transferring the data into the vector registers in col.1, lines 51-58, col.3, lines 29-32, see also fig.5 [main storage]),

b) at least one general purpose register (see the vector registers VRs in fig.5) , and

c) processor circuitry for executing one or more instructions (see load/store instruction format in fig.4b), at least one of the one or more instructions for transferring data elements between the memory (main memory) and the at least one general purpose register (VR) wherein one of the one or more instructions specifies: (a) a first offset [1] between data elements within a first portion of successive data elements in the memory (see data elements A (I-1), A(I) A(I+1) in col.13, lines 30-35); (b) a first number of data elements [L] to be transferred between the memory and the at least one GPR (see fig.4b [L]); and (c) a second offset [D1] between the first portion [starting element ] (see

start element number specified in OP instruction in fig.4 (b) [D1]) and a second portion [element start at D1] .

4. As to the newly amended feature of memory does not include the general purpose register (see memory [201] and general purpose registers [VR0] [VR1] in fig.5

See col.13, lines 29-67 for following illustrations.

first offset : offset between any two A(I)s is 1

second offset : offset between A(I-1) and A(I) is D1-0 = D1

0 D1-0

starting element element at D1

A(I-1)----------A(I)----------A(I+1)----------

5. As to claim 2, Inagami VIR (the distance or length) also specify the size of a data element (see VIR value when the L=1).

6. As to claim 6, Inagami also included total number of data elements to be transferred (sse L in fig.4, see col.4, lines 54-56).

7. AS to claim 7,17, Inagami 's one of one or more instructions also transferred between the memory and both registers (see the transfer between the memory and plurality of registers in col.3, lines 28-33).

8. As to claim 10, 19,20,21,25, Inagami also specified number of data elements to be transferred between memory and each register (see L in col.4, lines 53-58, see fig.4b [L]).

9. As to claims 12,27, Inagami also used the offset (see D1) once while transferring the first number o f data elements (see D1 with corresponding L in col.4, lines 45-65).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3-5 , 18, 34,37, 40,43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagami (4,760,545) in view of Omoda et al. (4,825,361) .

11. As to claims 3-5 , 18, 34,37, 40,43, Inagami did not specifically tech the specified size of data element separate and independent from the specifying size of data in memory as claimed . However, Omoda disclosed that the size of the vector elopement specified in the memory was independent from the size in the register (see col.). It would have been obvious tom one of ordinary skill in the art to use Omoda in Inagami for specifying the intendment and separate size in memory form the size specified in the register as claimed because the use of Omoda could provide the control ability of Inagami to adapt to different vector data element size based on the system

requirements, such as the specific data width of the system bus, and therefore it would allow Inagami the flexibility to rearrange the vector data element based on the bus width, and because Inagami also taught

12. Claims 13, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagami (4,760,545) in view of Betker et al. (6,052,766).

13. As to claims 13,28, limitations of parent claims already discussed above not be repeated herein. Inagami did not specifically show the circular buffer as claimed . However, Betker taght a vector system including a circular buffer (see col.15, lines 1-18). It would have been obvious to one of ordinary skill in the art to use Betker in Inagami for including the circular buffer as clamed because the use of Betker could provide Inagami the ability to reuse the data elements in a repeated cycle, therefore, increasing the data storage access in a predefined sequence, and it could be done by predefining the port width of circular buffer of Betker into the configuration file of Inagame so that the particular R/W port of Betker circular buffer could be recognized by Inagami, and because Inagami's teaching of the vector iteration (see the iterated do loop of vector operation in fig.1) was a suggestion of the need for providing a buffer in a predetermined loop sequence , or the like, for sorting vector data elements for respective values of the loop control variable accessed directly for the do loop vector operation, thereby minimized the overall latency due to the circuit overheads, and for doing so, provided a motivation.

14. Claim 15, 30, 31, 32 ,33,35,36,38,39,41,42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inagami (4,760,545) in view of Blomgren et al. (6,898,691)

15. As to claims 15, 30, 31,32,33, 35, 38, 41, limitation of parent 16 have been discussed above. Inagami taught at least :

a) a memory for storing operands (see the main storage for storing the vector data elements and transferring the data into the vector registers in col.1, lines 51-58, col.3, lines 29-32),

b) at least one general purpose register (see the vector registers VR) , and

c) processor circuitry for executing one or more instructions (see load/store instruction format in fig.4b), at least one of the one or more instructions for transferring data elements between the memory (main memory) and the at least one general purpose register (VR) wherein one of the one or more instructions specifies: (a) a first offset [1] between data elements within a first portion of successive data elements in the memory; (b) a first number of data elements [L] to be transferred between the memory and the at least one GPR; and (c) a second offset [D1] between the first portion A[I-1] and a second portion A[I] of data elements (e.g. see fig.5 data elements in [VR], See col.13, lines 29-67 for A(I-1) A(I) and A(I+1)).

16. As to the newly amended feature of memory does not include the general purpose register (see memory [201] and general purpose registers [VR0] [VR1] in fig.5

17. Inagami did not specifically show his instruction specified a radix specifier for implementing the data element transfer in bit reverse order (claim 16, 30, 31, reverse order for claims 32, 35 , 41) as claimed. However, Blomgren taught a vector system including instruction for specifying a radix and transferring data element in reverse order (see the radix reversal order col.9, lines 27-59, col.11, lines 34-42, see also col.6, ,lines 6-18 for transfer between memory and vector registers). It would have been obvious to one of ordinary skill in the art to use Blomgren in Inagami for including the radix for implementing the reversed bit transfer as clamed because the use of Blomgren could provide Inagami the capability to accept data in a predefined set of order , therefore, increasing the ability of Inagami for processing the vector operation with higher degree of complexity, and because one of ordinary skill in the art should be able to recognize the use of Blomgren into Inagami as Inagami sought the possibility to avoid reading and writing from a main memory (known to be slow) and effected the processing that the of the vector data referenced only once (see col.15, lines 35-52) , and Blomgren was looking for the solution for reducing the number of independent memory transfer (i.e. read/write) and improve the performance (col.2, lines 6-15), therefore, both Inagami and Blomgren were directed to the same problem, and in doing so, provided motivation.

18. As to applicant's remarks that no teaching or suggestion of using a radix specifier within an instruction itself, Blomgren clearly taught a block4 instruction for performing radix 4-bit reversal (see col.11, lines 31-42).

19. As to the multiple use of block4 instruction, applicant is reminded that multiple use of a single block4 instruction is different than multiple instructions. Multiple use is not the same as multiple instructions.

20. As to the remark by applicant that Blomgren did not have transfer of register and memory, Blomgren was looking for the solution for reducing the number of independent memory transfer (i.e. read/write) and improve the performance (col.2, lines 6-15), therefore Blomgren indicated the applicability for transfer in memory in addition to the data transfer present in the registers.

21. As to claims 36,39, 42 Inagami also included total number of data elements to be transferred (see L in fig.4, see col.4, lines 54-56).

22. Claims 8,9 ,23 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of specifying a total number of data elements to be transferred between the memory and both the first and second registers.

23. Claims 11 ,24 , 26 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record

further teaches the combined features of filing at least a portion of any remaining bit locations either predetermined value if the total number of data elements transferred does not completely fill the second register.

24. Claims 14 , 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the specifier the second offset used mo0re than once if the first number of data elements to be transferred is larger that twice the first portion of the dale elements to be transferred.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*21 Century Strategic Plan*

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